

1 4. The method of forming a thin film transistor of claim 1
2 comprising doping the source region and the drain region in a single
3 step.

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5 5. A method of forming a thin film transistor over a substrate
6 comprising the following steps:

7 providing a layer of semiconductive material from which a source
8 region, a drain region and a channel region of a thin film transistor
9 are to be formed; and

10 conductively doping the source region and the drain region of the
11 semiconductive material layer while preventing conductivity doping of the
12 channel region of the semiconductive material layer, such source region
13 doping and such drain region doping being conducted without any
14 masking of the channel region by any separate masking layer.

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16 6. The method of forming a thin film transistor of claim 5
17 wherein the source region and the drain region are oriented parallel
18 relative to one another, the channel region being oriented substantially
19 perpendicularly relative to the source and drain regions.

1 7. The method of forming a thin film transistor of claim 5
2 wherein the source region and the drain region are oriented substantially
3 parallel with one another and the substrate, the channel region being
4 oriented substantially perpendicularly relative to the substrate and the
5 source and drain regions.

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7 8. The method of forming a thin film transistor of claim 5
8 comprising doping the source region and the drain region in a single
9 step.

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1 9. A method of forming a thin film transistor comprising the
2 following steps:

3 providing a substrate having a node to which electrical connection
4 is to be made;

5 providing a first electrically insulative dielectric layer over the
6 substrate;

7 providing an electrically conductive gate layer over the first
8 dielectric layer;

9 providing a second electrically insulative dielectric layer over the
10 electrically conductive gate layer;

11 providing a contact opening through the second dielectric layer,
12 the electrically conductive gate layer and the first dielectric layer; the
13 contact opening defining projecting sidewalls;

14 providing a gate dielectric layer within the contact opening
15 laterally inward of the contact opening sidewalls;

16 - providing a layer of semiconductive material over the second
17 dielectric layer and within the contact opening against the gate dielectric
18 layer and in electrical communication with the node; the semiconductive
19 material within the contact opening defining an elongated and outwardly
20 extending channel region the electrical conductance of which can be
21 modulated by means of the adjacent electrically conductive gate and
22 gate dielectric layers; and

1 conductively doping the semiconductive material layer lying
2 outwardly of the contact opening to form one of a source region or a
3 drain region of a thin film transistor.

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5 10. The method of forming a thin film transistor of claim 9
6 wherein the step of providing the semiconductive material layer
7 comprises only partially filling the contact opening to define an annulus
8 within the contact opening, the channel region comprising the annulus.

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10 11. The method of forming a thin film transistor of claim 9
11 wherein the projecting sidewalls are provided to be substantially
12 perpendicular relative to the substrate.

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14 12. The method of forming a thin film transistor of claim 9
15 wherein the step of providing the semiconductive material layer
16 comprises only partially filling the contact opening to define an annulus
17 within the contact opening, the channel region comprising the annulus,
18 and wherein the projecting sidewalls are provided to be substantially
19 perpendicular relative to the substrate.

13. The method of forming a thin film transistor of claim 9 wherein the step of providing the gate dielectric layer comprises:

depositing a gate dielectric layer over the second dielectric layer and to within the contact opening, the deposited gate dielectric layer less than completely filling the contact opening; and

anisotropically etching the gate dielectric layer to define a gate dielectric layer annulus within the contact opening.

14. The method of forming a thin film transistor of claim 9 wherein the layer of semiconductive material is provided to completely fill the contact opening.

15. The method of forming a thin film transistor of claim 9 wherein the step of providing the gate dielectric layer comprises:

depositing a gate dielectric layer over the second dielectric layer and to within the contact opening, the deposited gate dielectric layer less than completely filling the contact opening; and

anisotropically etching the gate dielectric layer to define a gate dielectric layer annulus within the contact opening; and

wherein the step of providing the semiconductive material layer comprises only partially filling the contact opening to define the channel region is the shape of an annulus within the contact opening.

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1 16. The method of forming a thin film transistor of claim 9
2 wherein the step of providing the gate dielectric layer comprises:

3 depositing a gate dielectric layer over the second dielectric layer
4 and to within the contact opening, the deposited gate dielectric layer
5 less than completely filling the contact opening; and

6 anisotropically etching the gate dielectric layer to define a gate
7 dielectric layer annulus within the contact opening;

8 wherein the step of providing the semiconductive material layer
9 comprises only partially filling the contact opening to define the channel
10 region is the shape of an annulus within the contact opening; and

11 wherein the projecting sidewalls are provided to be substantially
12 perpendicular relative to the substrate.

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14 17. The method of forming a thin film transistor of claim 9
15 wherein the one region is provided run substantially parallel with the
16 substrate.

1 18. The method of forming a thin film transistor of claim 9
2 wherein,

3 the step of providing the contact opening comprises:

4 providing an initial contact opening through the second
5 electrically conductive layer to the electrically conductive
6 gate layer;

7 providing a preliminary electrically insulative layer over
8 the second dielectric layer and to within the initial contact
9 opening, the deposited preliminary electrically insulative layer
10 less than completely filling the initial contact opening; and

11 anisotropically etching the primary electrically insulative
12 layer to define an insulative spacer within the initial contact
13 opening; and

14 the step of providing the gate dielectric layer comprises:

15 providing a secondary contact through the gate layer
16 and the first dielectric layer using the insulative spacer as
17 an etching mask;

18 providing a secondary electrically insulative layer over
19 the second dielectric layer, the insulative spacer and to
20 within the secondary contact opening, the deposited
21 secondary electrically insulative layer less than completely
22 filling the secondary contact opening; and
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1 anisotropically etching the secondary electrically
2 insulative layer to define a gate dielectric layer annulus
3 within the secondary contact opening.
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5 19. A product produced by the process of claim 18.
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7 20. A thin film transistor comprising:
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9 a thin film transistor layer having a source region, a channel
10 region and a drain region; and
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12 a gate in proximity to the thin film channel region, the gate
13 comprising an annulus which encircles the thin film channel region.
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15 21. The thin film transistor of claim 20 wherein the gate
16 annulus is longitudinally elongated.
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18 22. The thin film transistor of claim 20 wherein at least one
19 of the source region or the drain region is elongated and the channel
20 region is elongated, the channel region being oriented substantially
21 perpendicularly relative to the one region.
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23 23. The thin film transistor of claim 20 wherein the source
24 region and the drain region are elongated and oriented parallel relative
to one another, the channel region being elongated and oriented
substantially perpendicularly relative to the source and drain regions.

24. The thin film transistor of claim 20 wherein the thin film transistor is provided relative to a supporting substrate, the gate annulus being longitudinally elongated and oriented substantially perpendicularly relative to the substrate.

25. A thin film transistor comprising:

a thin film transistor layer having a source region, a channel region and a drain region; the thin film channel region comprising an annulus; and

a gate in proximity to the thin film channel annulus.

26. The thin film transistor of claim 25 wherein the channel annulus is longitudinally elongated.

27. The thin film transistor of claim 25 wherein at least one of the source region or the drain region is elongated and the channel region is elongated, the channel region being oriented substantially perpendicularly relative to the one region.

28. The thin film transistor of claim 25 wherein the source region and the drain region are oriented parallel relative to one another, the channel region being oriented substantially perpendicularly relative to the source and drain regions.

1 29. The thin film transistor of claim 25 wherein the thin film
2 transistor is provided relative to a supporting substrate, the channel
3 annulus being longitudinally elongated and oriented substantially
4 perpendicularly relative to the substrate.

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6 30. A thin film transistor comprising:
7 a thin film transistor layer having a source region, a channel
8 region and a drain region; the thin film channel region comprising an
9 annulus; and
10 a gate in proximity to the thin film channel annulus, the gate
11 comprising an annulus which surrounds the thin film channel annulus.

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13 31. The thin film transistor of claim 30 wherein the channel
14 annulus and the gate annulus are longitudinally elongated.

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16 32. The thin film transistor of claim 30 wherein at least one
17 of the source region or the drain region is elongated and the channel
18 region is elongated, the channel region being oriented substantially
19 perpendicularly relative to the one region.

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21 33. The thin film transistor of claim 30 wherein the source
22 region and the drain region are oriented parallel relative to one
23 another, the channel region being oriented substantially perpendicularly
24 relative to the source and drain regions.

1 34. The thin film transistor of claim 30 wherein the thin film
2 transistor is provided relative to a supporting substrate, the channel
3 annulus and the gate annulus being longitudinally elongated and oriented
4 substantially perpendicularly relative to the substrate.

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6 35. A thin film transistor comprising:

7 a base layer having a locally substantially planar outer surface;

8 a thin film transistor layer provided outwardly of the base layer
9 outer surface; the thin film layer having a source region, a channel
10 region and a drain region; at least one of the thin film source region
11 or the thin film drain region being elongated and oriented substantially
12 parallel with the base layer outer surface; the thin film channel region
13 consisting essentially of a region elongated in a direction substantially
14 perpendicular to the base layer outer surface; and

15 a gate in proximity to the thin film channel region, the gate
16 being elongated in a direction substantially perpendicular to the base
17 layer outer surface along the thin film channel region.